WHAT IS CLAIMED IS:

1. A voltage controlled oscillator (VCO) having a VCO output signal with selectable frequency ranges comprising:

M inverting circuits coupled in series forming M+1 nodes N(1) to N(M+1), wherein M is an odd integer number greater than three;

M voltage controlled feedforward inverting (VCFF) circuits, each VCFF(J) having a control voltage input, a signal input I(J) coupled to a corresponding node N(J), where J is a number (1 to M), and a signal output X(J), the first number (M-2K) of the signal outputs X(1) to X(M-2K) are coupled to corresponding nodes N(4) to N(M-2K+3);

first circuitry for selectively coupling a first feedback signal selected from signals on K of first candidate nodes (N(M+1) to N(M-2K+3)), to node N(1), wherein K is an integer number greater than or equal to two and less than or equal to (M-5), in response to the one or more latched select signals, thereby generating the VCO output signal;

second circuitry for selectively coupling a second feedback signal from signals on K second candidate outputs X(M-1) to X(M-2K+1) to node N(2) in response to the one or more latched select signals; and

third circuitry for selectively coupling a third feedback signal from signals on K third candidate outputs X(M) to X(M-2K+2) to node N(3) in response to the one or more latched select signals.

2. The VCO of claim 1, wherein the one or more latched select signals are generated by latching asynchronous select signals when the first feedback signal coupled to node N(1) from a presently selected node N(Pr) from nodes N(M+1) to N(M-2K+3) setting of a present frequency range of the VCO has the same logic state

as a signal on a next selected node N(Pn) setting a next frequency range, thereby assuring switching from the present frequency range to the next frequency range of the VCO occurs glitch free.

3. The VCO of claim 1, wherein the number of candidate outputs K is limited by the requirement that all of the K first candidate outputs have the same logic state for a time period necessary to generate a new latched select signal and to switch between a present and a next candidate output.

4. The VCO of claim 1, wherein the VCO output signal is generated at node N(1) or node N(M+1).

5. The VCO of claim 1, wherein the one or more latched select signals are generated by latching asynchronous select signals on a state of a signal selected from signals on one of the K first candidate nodes N(M+1) to N(M-2K+3).

6. A phase locked loop circuit for generating an output clock signal with a selectable frequency range and a frequency that is a multiple number N times the frequency of a reference clock signal comprising:

a voltage controlled oscillator (VCO) generating the output clock signal with a frequency range set by one or more frequency range select signals, a frequency divider for frequency dividing the output clock signal by N generating a frequency divided clock signal, a phase frequency detector for comparing the frequency divided clock signal to the reference clock signal and generating a phase/frequency error signal, circuitry for converting the phase/frequency error signal to the control voltage, the VCO having M of inverting circuits (IVC) coupled in series forming M+1 nodes N(1) to N(M+1), wherein M is an odd integer number including greater than three, the VCO having:

M voltage controlled feedforward inverting (VCFF) circuits, each VCFF(J) having a control voltage input, a signal input I(J) coupled to a corresponding node N(J), where J is a number (1 to M), and a signal output X(J), the first number (M-2K) of the signal outputs X(1) to X(M-2K) are coupled to corresponding nodes N(4) to N(M-2K+3);

first circuitry for selectively coupling a first feedback signal selected from signals on K of first candidate nodes (N(M+1) to N(M-2K+3)), to node N(1), wherein K is an integer number greater than or equal to two and less than or equal to (M-5), in response to the one or more latched select signals, thereby generating the VCO output signal;

second circuitry for selectively coupling a second feedback signal from signals on K second candidate outputs X(M-1) to X(M-2K+1) to node N(2) in response to the one or more latched select signals; and

third circuitry for selectively coupling a third feedback signal from signals on K third candidate outputs X(M) to X(M-2K+2) to node N(3) in response to the one or more latched select signals.

7. The phase locked loop circuit of claim 6, wherein the one or more latched select signals are generated by latching asynchronous select signals when the first feedback signal coupled to node N(1) from a presently selected node N(Pr) from nodes N(M+1) to N(M-2K+3) setting of a present frequency range of the VCO has the same logic state as a signal on a next selected node N(Pn) setting a next frequency range, thereby assuring switching from the present frequency range to the next frequency range of the VCO occurs glitch free.

8. The phase locked loop circuit of claim 6, wherein the number of candidate outputs K is limited by the requirement that all of the K first candidate outputs have the same logic state for a time period necessary to generate a new latched select signal and to switch between a present and a next candidate output.

9. The phase locked loop circuit of claim 6, wherein the output clock signal is generated at node N(1) or node N(M+1).

10. The phase locked loop circuit of claim 6, wherein the one or more latched select signals are generated by latching asynchronous select signals on a state of a signal selected from signals on one of the K first candidate nodes N(M+1) to N(M-2K+3).

11. A data processing system comprising:

a central processing unit (CPU) clocked by a CPU clock signal;

a random access memory (RAM);

a read only memory (ROM);

an I/O adapter;

a bus system coupling said CPU to said ROM, said communications adapter, said I/O adapter, and said RAM, wherein the CPU clock signal is generated by phase locked loop circuitry with a frequency a multiple number N times the frequency of a reference clock signal comprising:

a voltage controlled oscillator (VCO) generating the output clock signal with a frequency range set by one or more frequency range select signals, a frequency divider for frequency dividing the output clock signal by N generating a frequency divided clock signal, a phase frequency detector for comparing the frequency divided clock signal to the reference clock signal and generating a phase/frequency error signal, circuitry for converting the phase/frequency error signal to the control voltage, the VCO having M of inverting circuits (IVC) coupled in series forming M+1 nodes N(1) to N(M+1), wherein M is an odd integer number including greater than three, the VCO having;

M voltage controlled feedforward inverting (VCFF) circuits, each VCFF(J) having a control voltage input, a signal input I(J) coupled to a corresponding node N(J), where J is a number (1 to M), and a signal output X(J), the first number (M-2K) of the signal outputs X(1) to X(M-2K) are coupled to corresponding nodes N(4) to N(M-2K+3);

first circuitry for selectively coupling a first feedback signal selected from signals on K of first candidate nodes (N(M+1) to N(M-2K+3)), to node N(1), wherein K is an integer number greater than or equal to two and less than or equal to (M-5), in

response to the one or more latched select signals, thereby generating the VCO output signal;

second circuitry for selectively coupling a second feedback signal from signals on K second candidate outputs X(M-1) to X(M-2K+1) to node N(2) in response to the one or more latched select signals; and

third circuitry for selectively coupling a third feedback signal from signals on K third candidate outputs X(M) to X(M-2K+2) to node N(3) in response to the one or more latched select signals.

12. The data processing system of claim 11, wherein the one or more latched select signals are generated by latching asynchronous select signals when the first feedback signal coupled to node N(1) from a presently selected node N(Pr) from nodes N(M+1) to N(M-2K+3) setting of a present frequency range of the VCO has the same logic state as a signal on a next selected node N(Pn) setting a next frequency range, thereby assuring switching from the present frequency range to the next frequency range of the VCO occurs glitch free.

13. The data processing system of claim 11, wherein the number of candidate outputs K is limited by the requirement that all of the K first candidate outputs have the same logic state for a time period necessary to generate a new latched select signal and to switch between a present and a next candidate output.

14. The data processing system of claim 11, wherein the output clock signal is generated at node N(1) or node N(M+1).

15. The data processing system of claim 11, wherein the one or more latched select signals are generated by latching asynchronous select signals on a state of a

signal selected from signals on one of the K first candidate nodes N(M+1) to N(M-2K+3).